AMENDMENTS TO THE SPECIFICATION

Please replace paragraph at page 3, line 13 with the following rewritten paragraph:

According to one aspect, the invention provides a method of fabricating a split gate flash memory cell. First, a substrate having a trench is provided, and a conductive [[stud]] line insulated from the substrate is formed in ~~the lower~~ a lower portion of the trench serving as a source line. Next, a source region is formed in the substrate adjacent to ~~the upper conductive stud~~ an upper portion of the conductive line. Next, an insulating layer is formed on the conductive [[stud]] line. Next, a conductive spacer is formed on the upper sidewall of the trench serving as a floating gate, protruding and insulated from the substrate. Next, an insulating stud is formed on the insulating layer, wherein the insulating stud is higher than the conductive spacer in height. Next, a first conductive layer is formed over the substrate ~~of the outside~~ adjacent to the conductive spacer, wherein the first conductive layer is insulated from the conductive spacer and the substrate, respectively. Next, a first insulating spacer is formed on the sidewall of the insulating stud to cover a part of the first conductive layer. Next, the first conductive layer is removed using the first insulating spacer as a mask to expose the substrate and the remaining conductive layer is used as a control gate. Finally, a drain region is formed in the exposed substrate.

Please replace paragraph at page 4, line 4 with the following rewritten paragraph:

According to another aspect, the invention provides a split gate flash memory cell. The memory cell includes a substrate having a trench, a conductive [[stud]] line disposed in ~~the lower~~ a lower portion of the trench and insulated from the substrate serving as a source line, a source region formed in the substrate adjacent to ~~the upper conductive stud~~ an upper portion of the conductive line, and an insulating layer disposed on the conductive [[stud]] line. A conductive spacer is disposed on the upper sidewall of the trench serving as a floating gate, protruding and insulated from the substrate. An insulating stud is disposed on the insulating layer, with the top thereof higher than that of the conductive spacer in height. A first conductive layer is disposed over the substrate ~~of the outside~~ adjacent to the conductive spacer serving as a control gate, and is insulated from the conductive spacer and the substrate, respectively. A

first insulating spacer disposed on the sidewall of the insulating stud covers the first conductive layer, and a drain region is formed in the substrate ~~of the outside~~ adjacent to the first conductive layer.

Please replace paragraph at page 6, line 8 with the following rewritten paragraph:

In FIG. 4, the conductive layer 216 in the trench 212 is etched back again to lower the conductive layer 216 below the insulating spacer 218. Subsequently, the liner oxide 214 between the insulating spacer 218 and the conductive layer 216 is removed by isotropic etching, such as wet etching, to expose a part of the substrate 200. The remaining conductive layer 216 in ~~the lower~~ a lower portion of the trench 212 forms a conductive [[stud]] line 216' serving as a source line insulated from the substrate 200 by the remaining liner oxide 214. Next, a conformable conductive layer 220, such as a doped polysilicon layer, is formed on the second mask layer 205 and the surface of the trench 212 by conventional deposition, such as CVD. Next, a doping region S is formed in the exposed substrate 200 of the trench 212 adjacent to ~~the upper conductive stud~~ an upper portion of the conductive line (source line) 216' by performing a high temperature drive-in process on the conductive layer 220, serving as a source region.

Please replace paragraph at page 6, line 23 with the following rewritten paragraph:

In FIG. 5, the conductive layer 220 over the conductive [[stud]] line 216' is etched back to leave a part of conductive layer 220 on the liner oxide 214 to make connection between the conductive [[stud]] line 216' and the doping region S. Thereafter, the insulating spacer 218 is removed, and a conformable insulating layer 222, such as high density plasma oxide (HDP oxide), is formed on the second mask layer 205 and the surface of the trench 212 by CVD. Here, the top and bottom of the insulating layer 222 are thicker than the sidewall of the insulating layer 222. Next, the trench 212 is filled with a photoresist layer 224 which is etched back to below the top of the trench 212.

Please replace paragraph at page 7, line 4 with the following rewritten paragraph:

In FIG. 6, the insulating layer [[224]] 222 on the sidewall of the trench 212 uncovered by the photoresist 224 is removed by isotropic etching, such as wet etching, using the photoresist layer 224 as a mask to expose the sidewall of the silicon nitride layer 208. Next, after the photoresist layer 224 is removed, the sidewall of the silicon nitride layer 208 is etched by isotropic etching, such as wet etching, using the remaining insulating layer 222' as a mask to expose the pad oxide 206 (etching stop layer) and form an opening 225 having a step profile.

Please replace paragraph at page 7, line 16 with the following rewritten paragraph:

In FIG. 7, the insulating layer 222' on the silicon nitride layer 208 and the sidewall of the trench 212 and the pad oxide 206 in the opening 225 are removed by isotropic etching, such as wet etching, to leave the insulating layer 222" on the conductive [[stud]] line 216' and expose the first mask layer 201 in the opening 225 and the substrate 200 in the trench 212, respectively. Next, an oxide layer 226 is formed on the exposed substrate 200 in the trench 212 by thermal oxidation. Next, a conductive layer 228, such as doped polysilicon, having a thickness about 200~400 Å is formed on the second mask layer 205 and the surface of the opening 225. Thereafter, a sacrificial layer 230, such as photoresist, is formed on the second mask layer 205 and filled into the opening 225 and the trench 212. Next, a part of the sacrificial layer 230 is removed to lower it below the top of the opening 225. Here, the top of the remaining sacrificial layer 230 is higher than the conductive layer 228 formed on the bottom of the opening 225 in height.

Please replace paragraph at page 8, line 6 with the following rewritten paragraph:

In FIG. 9, after the remaining sacrificial layer 230is removed, the conductive layer 228 is etched back by anisotropic etching, such as dry etching, to expose the insulating layer 222" and form a conductive spacer 228'on the sidewall of ~~the upper~~ an upper portion of the trench 212 protruding the top of the substrate 200. Here, the conductive spacer 228' having a tip portion is used as a floating gate, and the tip portion discharges during erasing. Moreover, the oxide layer 226 is used as a gate oxide. Next, an insulating layer 232, such as oxide, is filled into the

opening 225 by conventional deposition, such as low-pressure CVD (LPCVD). Subsequently, the insulating layer 232 is lowered below the top of the second mask layer 205. Next, a cap layer 234, such as silicon oxynitride or polysilicon, is deposited on the second mask layer 205 and the insulating layer 232. Thereafter, the excess cap layer 232 on the second mask layer 205 is removed by CMP.

Please replace paragraph at page 9, line 3 with the following rewritten paragraph:

FIGS. 12-15 are cross-sections showing a method of forming a control gate on the substrate 200 ~~of the outside~~ adjacent to the floating gate 228'.

Please replace paragraph at page 9, line 16 with the following rewritten paragraph:

In FIG. 13, the exposed conductive layer 238 is etched using the photoresist layer 240 as a mask to leave the conductive layer 238 over the substrate 200 ~~of the outside~~ adjacent to the floating gate 228'. The conductive layer 238 is insulated from the floating gate 228' and the substrate 200 by the oxide layer 236.

Please replace paragraph at page 11, line 3 with the following rewritten paragraph:

Also, FIG. 19 is a cross-section showing the structure of the split gate flash memory cell according to the present invention. The memory cell includes a substrate 200, such as a silicon wafer, having a trench. A conductive [[stud]] line 216', such as polysilicon, is disposed in ~~the lower~~ a lower portion of the trench serving as a source line. The source line 216' is insulated from the substrate 200 by an oxide layer 226.

Please replace paragraph at page 11, line 10 with the following rewritten paragraph:

A source region S is formed in substrate 200 adjacent to ~~the upper~~ an upper portion of the source line 216'. A conductive spacer 228' is disposed on the sidewall of ~~the upper~~ an upper portion of the trench and protrudes from the top of the substrate 200 serving as a floating gate. The floating gate 228' is insulated from the substrate 200 by the gate oxide 226.

Please replace paragraph at page 11, line 16 with the following rewritten paragraph:

The floating gate 228' is insulated from the source line 216' by an insulating layer 222", such as HDP oxide. An insulating stud 232' is disposed on the insulating layer 222". A conductive layer 238', such as doped polysilicon, is disposed on the substrate 200 ~~of the outside~~ adjacent to the floating gate 228' serving as a control gate. The control gate 238' is insulated from the floating gate 228' and the substrate 200 by gate oxide 236'.

Please replace paragraph at page 11, line 23 with the following rewritten paragraph:

An insulating spacer 244 is disposed on the sidewall of the insulating stud 232' and an insulating spacer 250 is disposed on the sidewall of the control gate 238'. These insulating spacers 244, 250 can be silicon nitride. A conductive layer 242, such as tungsten silicide, is disposed between the insulating spacer 244 and the control gate 238'. A drain region D is formed in the substrate 200 ~~of the outside~~ adjacent to the control gate 238'.

Please replace the Abstract with the following rewritten Abstract as shown on the following page: